AMENDMENTS TO THE CLAIMS

Claims 1-14. (Canceled)

15. (Previously Presented) A method for forming a semiconductor device comprising:

forming a first group of gate electrodes on a first region of a substrate so that the first group of gate electrodes are densely arranged;

forming a second group of gate electrodes on a second region of the substrate so that the second group of gate electrodes are sparsely arranged;

forming a first dielectric film as a single layer on the first region and the second region of the substrate on which the gate electrodes are formed so that the first dielectric film fills entire spaces between the gate electrodes;

planarizing the first dielectric film;

forming a second dielectric film on the first dielectric film, the second dielectric film having an etching rate different from an etching rate of the first dielectric film; and then

forming contact holes to a uniform depth through the first dielectric film and the second dielectric film,

wherein an entire surface of the first dielectric film is continuous and higher than a top surface of the gate electrodes just prior to planarizing the first dielectric film, and

wherein planarizing the first dielectric film results in the first dielectric film having a uniform thickness at those portions through which said contact holes are formed.

16. (Previously presented) The method of claim 15, further comprising planarizing the second dielectric film before forming the contact.

17. (Previously presented) The method of claim 15, wherein the first dielectric film includes phosphorus.

Claims 18-21. (Canceled)

22. (Previously presented) The method of claim 15, wherein the contact is connected to the substrate or a corresponding one of the gate electrodes.

Claim 23. (Canceled)

24. (Previously presented) The method of claim 15, wherein a distance between at least two adjacent ones of the gate electrodes formed on the first region is 0.3 μm or less.

Claim 25 (Canceled)

26. (Previously presented) The method of claim 15, further comprising heating the first dielectric film before the planarizing of the first dielectric film and after the forming of the first dielectric film.

27. (Previously presented) A method for forming a semiconductor device comprising:

forming a first group of interconnections on a first region of a substrate so that the first group of interconnections are densely arranged;

forming a second group of interconnections on a second region of the substrate so that the second group of interconnections are sparsely arranged;

forming a first dielectric film on the substrate;

planarizing the first dielectric film;

forming a second dielectric film on the first dielectric film, the second dielectric film having an etching rate different from an etching rate of the first dielectric film; and then

forming contact holes to a uniform depth through the first dielectric film and the second dielectric film,

wherein an entire surface of the first dielectric film is continuous and higher than a top surface of the interconnections just prior to planarizing the first dielectric film, and

wherein planarizing the first dielectric film results in the first dielectric film having a uniform thickness at those portions through which said contact holes are formed.

28. (Previously presented) The method of claim 27, wherein a distance between at least two adjacent ones of the interconnections formed on the first region is 0.3 μm or less.

29. (Previously presented) A method for forming a semiconductor device comprising:

forming a plurality of interconnections on a substrate, the interconnections including first interconnections and a second interconnection, the first interconnections having a width different than a width of the second interconnection;

forming a first dielectric film on the substrate;

planarizing the first dielectric film;

forming a second dielectric film on the first dielectric film, the second dielectric film having an etching rate different from an etching rate of the first dielectric film; and then

forming contact holes to a uniform depth through the first dielectric film and the second dielectric film,

wherein an entire surface of the first dielectric film is continuous and higher than a top surface of the interconnections just prior to planarizing the first dielectric film, and

wherein planarizing the first dielectric film results in the first dielectric film having a uniform thickness at those portions through which said contact holes are formed.

30. (Previously presented) The method of claim 29, wherein the first dielectric film includes phosphorus.

31. (Previously presented) The method of claim 29, further comprising heating the first dielectric film before the planarizing the first dielectric film.

32. (Previously Presented) A method for forming a semiconductor device comprising:

forming a first group of gate electrodes on a first region of a substrate so that the first group of gate electrodes are densely arranged;

forming a second group of gate electrodes on a second region of the substrate so that the second group of gate electrodes are sparsely arranged;

forming a first dielectric film as a single layer on the first region and the second region of the substrate on which the gate electrodes are formed so that the first dielectric film fills entire spaces between the gate electrodes, the first dielectric film including phosphorus;

heating the first dielectric film;

planarizing the first dielectric film after the heating of the first dielectric film;

forming a second dielectric film on the planarized first dielectric film, the second dielectric film comprising a non-doped oxide film; and then

forming contact holes to a uniform depth through the first dielectric film and the second dielectric film,

wherein planarizing the first dielectric film results in the first dielectric film having a uniform thickness at those portions through which said contact holes are formed.

33. (Previously presented) The method of claim 32, wherein a distance between at least two adjacent gate electrodes formed on the first region is 0.3 μm or less.

Claim 34. (Canceled)

35. (Previously Presented) A method for forming a semiconductor device comprising:

forming a first gate electrode, a second gate electrode adjacent the first gate electrode, and a third gate electrode adjacent the second gate electrode, on a substrate;

forming a first dielectric film as a single layer on the substrate so that the first dielectric film fills an entire space between the first and second gate electrodes and an entire space between the second and third gate electrodes;

planarizing a surface of the first dielectric film;

forming a second dielectric film on the surface of the first dielectric film, the second dielectric film having an etching rate different from an etching rate of the first dielectric film; and then

forming contact holes to a uniform depth through the first dielectric film and the second dielectric film;

wherein a distance between the first gate electrode and the second gate electrode is greater than a distance between the second gate electrode and the third gate electrode, and

wherein an entire surface of the first dielectric film is continuous and higher than a top surface of the first, second and third gate electrodes just prior to planarizing the first dielectric film, and

wherein planarizing the surface of the first dielectric film results in the first dielectric film having a uniform thickness at those portions through which said contact holes are formed.

36. (Previously presented) The method of claim 35, wherein the first dielectric film includes phosphorus.

37. (Previously presented) The method of claim 35, wherein the second dielectric film is a non-doped oxide film.

38. (Previously presented) The method of claim 35, wherein the contact is connected to the substrate, or to one of the first, second and third gate electrodes.

39. (Previously presented) The method of claim 35, wherein the distance between the second gate electrode and the third gate electrode is 0.3 μm or less.

40. (Previously presented) The method of claim 35, further comprising planarizing the second dielectric film before forming the contact.

41. (Previously presented) The method of claim 35, further comprising heating the first dielectric film before the planarizing of the first dielectric film.

42. (Previously presented) The method of claim 35, wherein a space between the first gate electrode and the second gate electrode, and a space between the second gate electrode and the third gate electrode, are filled with the first dielectric film.

43. (Previously presented) The method of claim 35, wherein the second dielectric film is formed on the first dielectric film before forming a precipitate on a surface of the first dielectric film, and after the planarizing of the first dielectric film.

44. (Previously presented) The method of claim 35, wherein the forming the second dielectric film on the first dielectric film is performed within 24 hours after the planarizing the first dielectric film.

45. (Previously presented) The method of claim 35, further comprising eliminating a precipitate on a surface of the first dielectric film after planarizing the first dielectric film.

46. (Previously presented) The method of claim 45, wherein the precipitate is eliminated by using a solution.

47. (Previously presented) The method of claim 35, wherein the second dielectric film is a non-doped oxide film.

48. (Previously presented) The method of claim35, wherein the contact is composed of a conductive film.

49. (Previously presented) The method of claim 15, wherein the second dielectric film is a non-doped oxide film.

50. (Previously presented) The method of claim 27, wherein the first dielectric film includes phosphorus.

51. (Previously presented) The method of claim 27, wherein the second dielectric film is a non-doped oxide film.

52. (Previously presented) The method of claim 32, wherein substantially an entire surface of the first dielectric film is continuous and higher than a top surface of the first, second and third gate electrodes just prior to planarizing the first dielectric film.

53. (Previously Presented) A method for forming a semiconductor device comprising:

forming a first interconnection, a second interconnection adjacent the first interconnection, and a third interconnection adjacent the second interconnection, on a substrate;

forming a first dielectric film as a single layer on the substrate so that the first dielectric film fills an entire space between the first and second interconnections and an entire space between the second and third interconnections;

planarizing a surface of the first dielectric film;

forming a second dielectric film on the surface of the first dielectric film, the second dielectric film having an etching rate different from an etching rate of the first dielectric film; and then

forming contact holes to a uniform depth through the first dielectric film and the second dielectric film;

wherein a distance between the first interconnection and the second interconnection is greater than a distance between the second interconnection and the third interconnection, and

wherein an entire surface of the first dielectric film is continuous and higher than a top surface of the first, second and third interconnections just prior to planarizing the first dielectric film, and

wherein planarizing the surface of the first dielectric film results in the first dielectric film having a uniform thickness at those portions through which said contact holes are formed.

54. (Previously presented) The method of claim 53, wherein the first dielectric film includes phosphorus.

55. (Previously presented) The method of claim 53, wherein the second dielectric film is a non-doped oxide film.

56. (Previously presented) The method of claim 53, wherein the contact is connected to the substrate or to one of the first, second and third interconnections.

57. (Previously presented) The method of claim 53, wherein the distance between the second interconnection and the third interconnection is 0.3 μm or less.

58. (Previously presented) The method of claim 53, further comprising planarizing the second dielectric film before forming the contact.

59. (Previously presented) The method of claim 53, wherein a space between the first interconnection and the second interconnection, and a space between the second interconnection and the third interconnection, are filled with the first dielectric film.

60. (Previously presented) The method of claim 15, wherein the first dielectric film is planarized by CMP.

61. (Previously presented) The method of claim 27, wherein the first dielectric film is planarized by CMP.

62. (Previously presented) The method of claim 29, wherein the first dielectric film is planarized by CMP.

63. (Previously presented) The method of claim 32, wherein the first dielectric film is planarized by CMP.

64. (Previously presented) The method of claim 35, wherein the first dielectric film is planarized by CMP.

65. (Previously presented) The method of claim 53, wherein the first dielectric film is planarized by CMP.

66. (New) The method of claim 15, wherein planarizing the first dielectric film results in the entire surface of the first dielectric film continuing to be higher than the top surface of the gate electrodes.

67. (New) The method of claim 27, wherein planarizing the first dielectric film results in the entire surface of the first dielectric film continuing to be higher than the top surface of the interconnections.

68. (New) The method of claim 29, wherein planarizing the first dielectric film results in the entire surface of the first dielectric film continuing to be higher than the top surface of the interconnections.

69. (New) The method of claim 32, wherein planarizing the first dielectric film results in the entire surface of the first dielectric film being higher than the top surface of the gate electrodes.

70. (New) The method of claim 35, wherein planarizing the first dielectric film results in the entire surface of the first dielectric film continuing to be higher than the top surface of the first, second and third gate electrodes.

71. (New) The method of claim 53, wherein planarizing the first dielectric film results in the entire surface of the first dielectric film continuing to be higher than the top surface of the first, second and third interconnections.

72. (New) The method of claim 15, wherein the first dielectric film is one selected from the group consisting of: a BPSG film, a PSG film, a BSG film, an oxide film which is formed by coating, a low dielectric constant film, an organic film, and a porous film.

73. (New) The method of claim 27, wherein the first dielectric film is one selected from the group consisting of: a BPSG film, a PSG film, a BSG film, an oxide film which is formed by coating, a low dielectric constant film, an organic film, and a porous film.

74. (New) The method of claim 29, wherein the first dielectric film is one selected from the group consisting of: a BPSG film, a PSG film, a BSG film, an oxide film which is formed by coating, a low dielectric constant film, an organic film, and a porous film.

75. (New) The method of claim 32, wherein the first dielectric film is one selected from the group consisting of: a BPSG film, a PSG film, a BSG film, an oxide film which is formed by coating, a low dielectric constant film, an organic film, and a porous film.

76. (New) The method of claim 35, wherein the first dielectric film is one selected from the group consisting of: a BPSG film, a PSG film, a BSG film, an oxide film which is formed by coating, a low dielectric constant film, an organic film, and a porous film.

77. (New) The method of claim 53, wherein the first dielectric film is one selected from the group consisting of: a BPSG film, a PSG film, a BSG film, an oxide film which is formed by coating, a low dielectric constant film, an organic film, and a porous film.

78. (New) The method of claim 15, wherein the second dielectric film is a TEOS film or a silicon nitride film.

79. (New) The method of claim 27, wherein the second dielectric film is a TEOS film or a silicon nitride film.

80. (New) The method of claim 29, wherein the second dielectric film is a TEOS film or a silicon nitride film.

81. (New) The method of claim 32, wherein the second dielectric film is a TEOS film or a silicon nitride film.

82. (New) The method of claim 35, wherein the second dielectric film is a TEOS film or a silicon nitride film.

83. (New) The method of claim 53, wherein the second dielectric film is a TEOS film or a silicon nitride film.

84. (New) The method of claim 15, wherein the etching rate of the first dielectric film is higher than the etching rate of the second dielectric film.

85. (New) The method of claim 27, wherein the etching rate of the first dielectric film is higher than the etching rate of the second dielectric film.

86. (New) The method of claim 29, wherein the etching rate of the first dielectric film is higher than the etching rate of the second dielectric film.

87. (New) The method of claim 32, wherein an etching rate of the first dielectric film is higher than an etching rate of the second dielectric film.

88. (New) The method of claim 35, wherein the etching rate of the first dielectric film is higher than the etching rate of the second dielectric film.

89. (New) The method of claim 53, wherein the etching rate of the first dielectric film is higher than the etching rate of the second dielectric film.